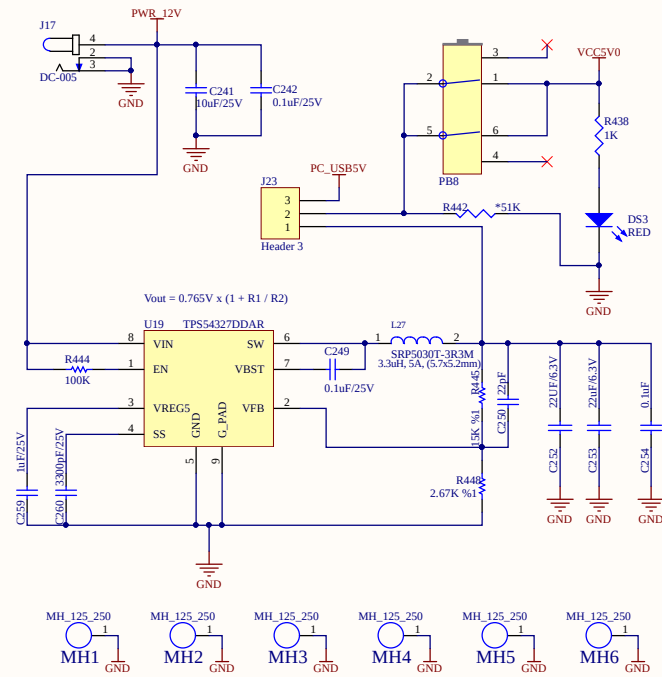
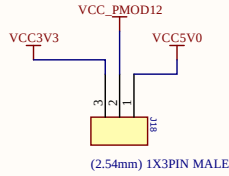
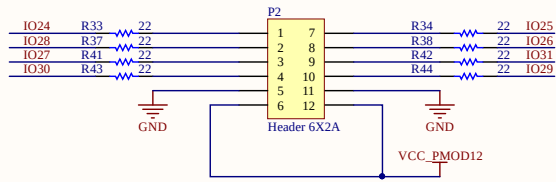


Power

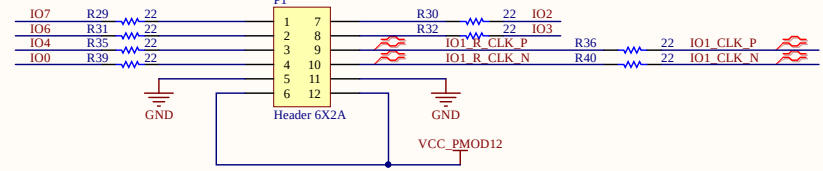


GPIO

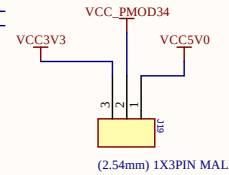
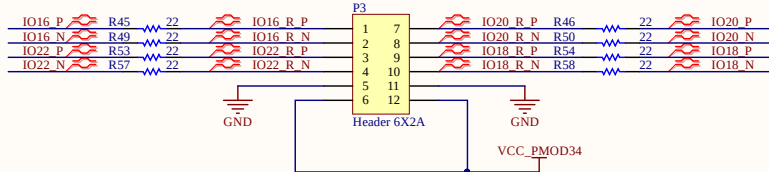
GPIO1



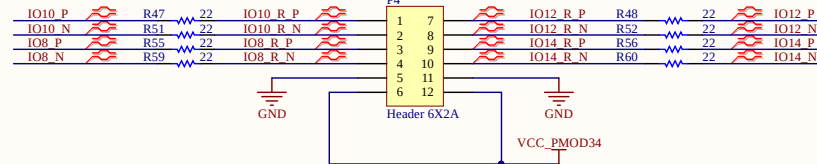
GPIO2



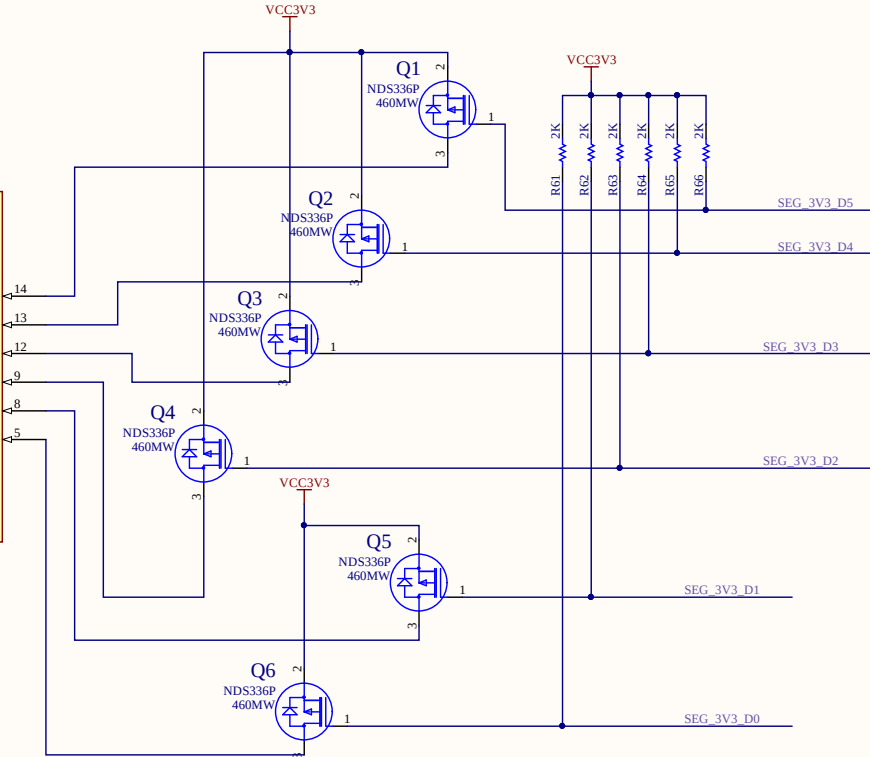
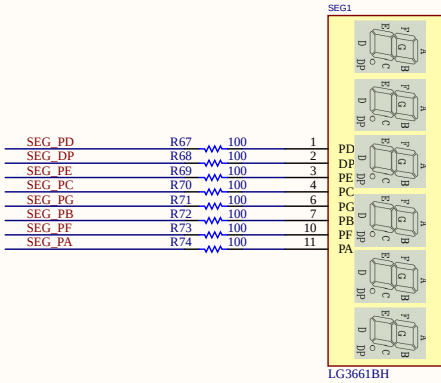
GPIO3



GPIO4

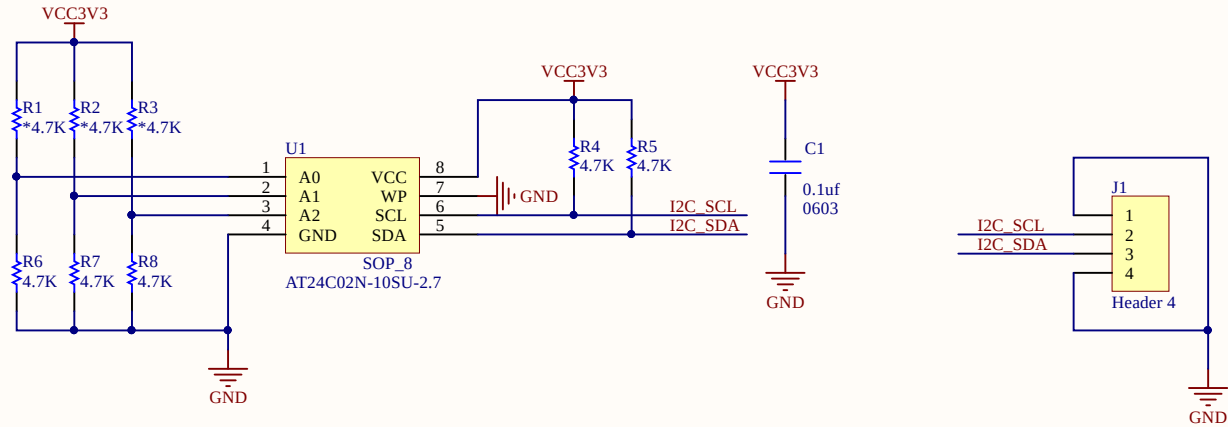


SEG

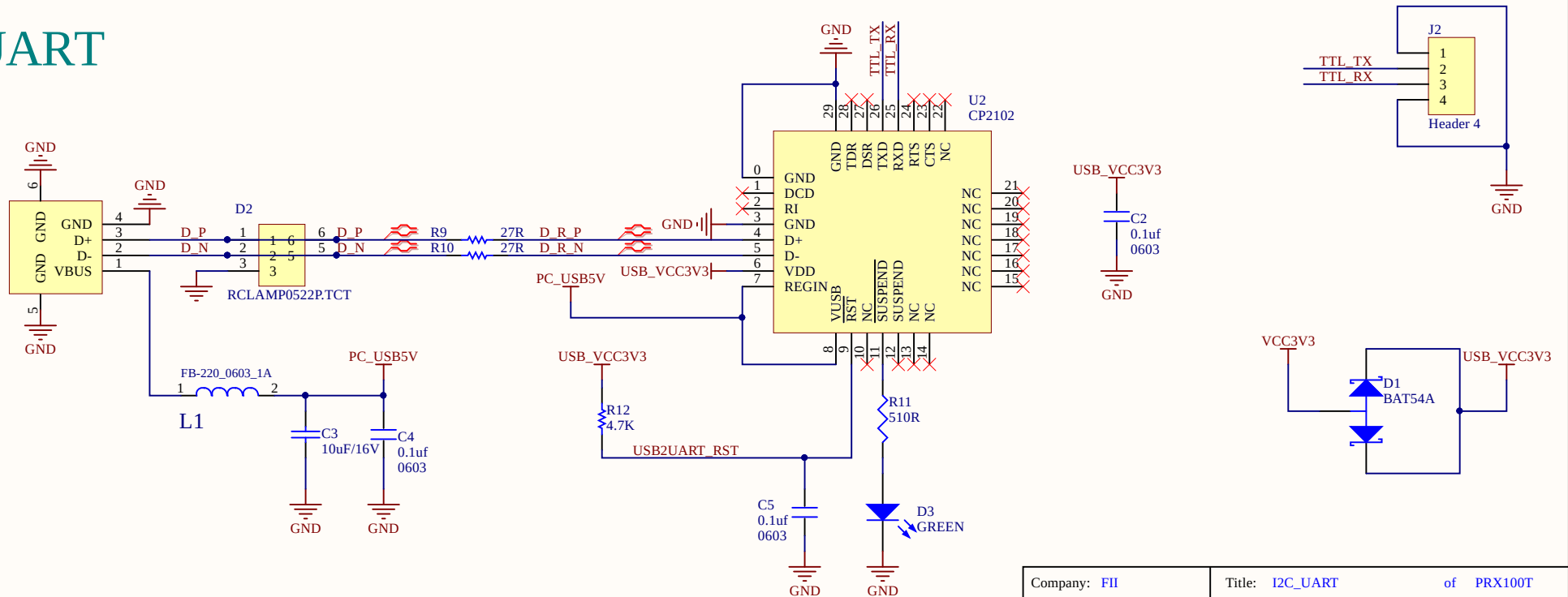


Company: FH	Title: SEG_GPIO of PRX100T
Date: 2021-07-05	Time: 6:06:49 PM
Engineer: RJ WG	Size: B
Revision: DDRV1.0	Sheet 03 of 25

I2C

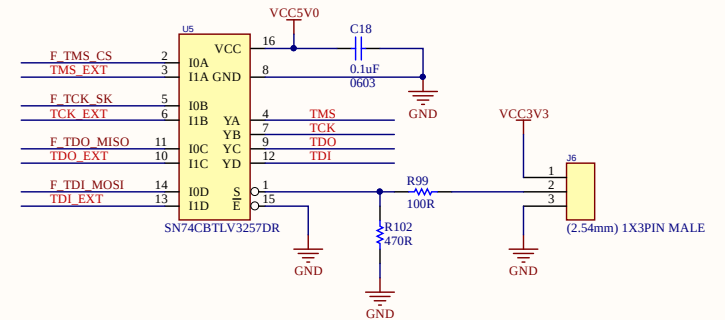
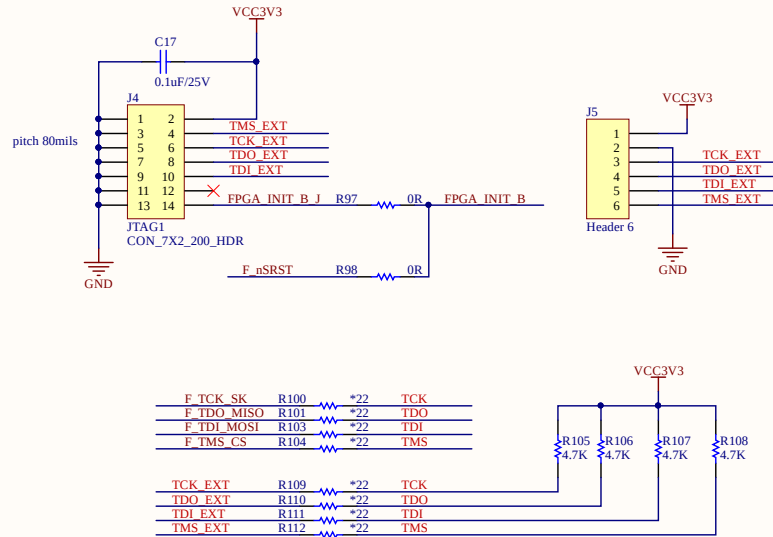


UART

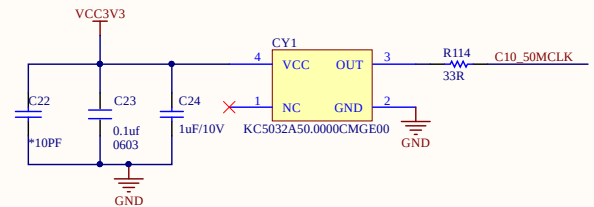
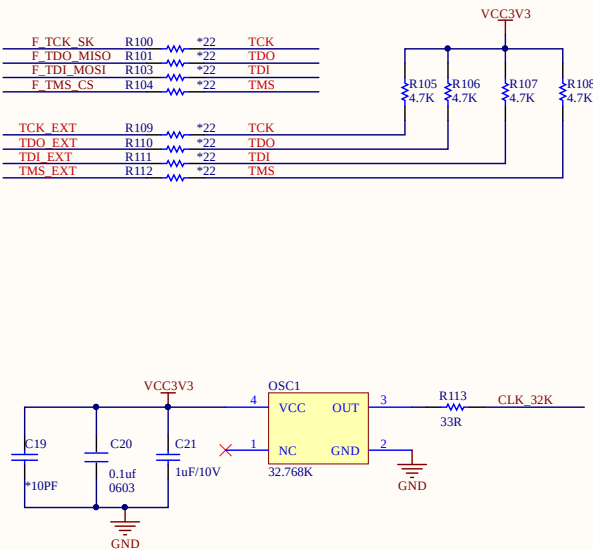


Company: FII	Title: I2C_UART	of PRX100T
Date: 2021-07-05	Time: 6:06:50 PM	Engineer: RJ WG
Revision: DDRV1.0	Sheet 05 of 25	Size: A4

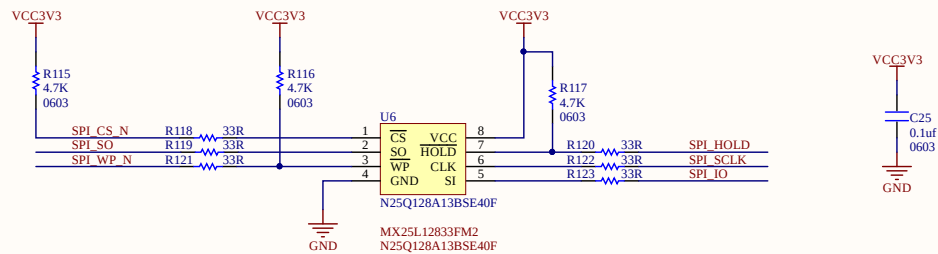
JTAG



XTAL



FLASH



Company: FH	Title: JTAG_OSC_FLASH of PRX100T
Date: 2021-07-05	Time: 6:06:50 PM
Revision: DDRV1.0	Sheet 07 of 25
Engineer: RJ WG	Size: B

U7A BANK13 1.5V

BANK 13

IO_0_13	U24	PL_DDR_RST_N
IO_L1P_T0_13	U25	PL_DDR_DQ3
IO_L1N_T0_13	U26	PL_DDR_DM0
IO_L2P_T0_13	V26	PL_DDR_DQ5
IO_L2N_T0_13	W26	PL_DDR_DQ7
IO_L3P_T0_DQS_13	AB26	PL_DDR_DQS0_P
IO_L3N_T0_DQS_13	AC26	PL_DDR_DQS0_N
IO_L4P_T0_13	W25	PL_DDR_DQ6
IO_L4N_T0_13	Y26	PL_DDR_DQ4
IO_L5P_T0_13	Y25	PL_DDR_DQ0
IO_L5N_T0_13	AA25	PL_DDR_DQ2
IO_L6P_T0_13	V24	PL_DDR_DQ1
IO_L6N_T0_VREF_13	W24	
IO_L7P_T1_13	AA24	PL_DDR_DQ15
IO_L7N_T1_13	AB25	PL_DDR_DQ13
IO_L8P_T1_13	AA22	PL_DDR_DQ9
IO_L8N_T1_13	AA23	PL_DDR_DQ11
IO_L9P_T1_DQS_13	AB24	PL_DDR_DQS1_P
IO_L9N_T1_DQS_13	AC24	PL_DDR_DQS1_N
IO_L10P_T1_13	V23	PL_DDR_DQ12
IO_L10N_T1_13	W23	PL_DDR_DQ10
IO_L11P_T1_SRCC_13	Y22	PL_DDR_DM1
IO_L11N_T1_SRCC_13	Y23	PL_DDR_DQ8
IO_L12P_T1_MRCC_13	U22	PL_DDR_DQ14
IO_L12N_T1_MRCC_13	V22	
IO_L13P_T2_MRCC_13	U21	PL_DDR_CK_P
IO_L13N_T2_MRCC_13	V21	PL_DDR_CK_N
IO_L14P_T2_SRCC_13	W21	PL_DDR_A10
IO_L14N_T2_SRCC_13	Y21	PL_DDR_CKE_0
IO_L15P_T2_DQS_13	T20	PL_DDR_ODT0
IO_L15N_T2_DQS_13	U20	PL_DDR_RAS_N
IO_L16P_T2_13	W20	PL_DDR_A0
IO_L16N_T2_13	Y20	PL_DDR_BA2
IO_L17P_T2_13	T19	PL_DDR_BA0
IO_L17N_T2_13	U19	PL_DDR_CAS_N
IO_L18P_T2_13	V19	PL_DDR_WE_N
IO_L18N_T2_13	W19	PL_DDR_A12
IO_L19P_T3_13	V18	PL_DDR_A1
IO_L19N_T3_VREF_13	W18	PL_DDR_BA1
IO_L20P_T3_13	T14	PL_DDR_A8
IO_L20N_T3_13	T15	PL_DDR_A13
IO_L21P_T3_DQS_13	T17	PL_DDR_A5
IO_L21N_T3_DQS_13	T18	PL_DDR_A3
IO_L22P_T3_13	U15	PL_DDR_A9
IO_L22N_T3_13	U16	PL_DDR_A7
IO_L23P_T3_13	U14	PL_DDR_A2
IO_L23N_T3_13	V14	PL_DDR_A6
IO_L24P_T3_13	V16	PL_DDR_A11
IO_L24N_T3_13	V17	PL_DDR_A4
IO_25_13	U17	

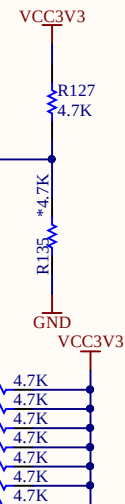
XC7A100T-2FGG676I

U7B BANK14 3.3V

BANK 14

IO_0_14	M19	LED1
IO_L1P_T0_D00_MOSI_14	R14	SPI IO
IO_L1N_T0_D01_DIN_14	R15	SPI SO
IO_L2P_T0_D02_14	P14	SPI WP_N
IO_L2N_T0_D03_14	N14	SPI HOLD
IO_L3P_T0_DQS_PUDC_B_14	P15	
IO_L3N_T0_DQS_EMCCLK_14	P16	LED2
IO_L4P_T0_D04_14	N16	LED3
IO_L4N_T0_D05_14	N17	LED0
IO_L5P_T0_D06_14	R16	SEG_3V3_D5
IO_L5N_T0_D07_14	R17	SEG_3V3_D4
IO_L6P_T0_FCS_B_14	P18	SPI CS_N
IO_L6N_T0_D08_VREF_14	N18	SEG_3V3_D3
IO_L7P_T1_D09_14	K25	SEG_3V3_D2
IO_L7N_T1_D10_14	K26	SEG_PA
IO_L8P_T1_D11_14	M20	SEG_PB
IO_L8N_T1_D12_14	L20	SEG_PC
IO_L9P_T1_DQS_14	L24	CPU TTDO
IO_L9N_T1_DQS_D13_14	L25	CPU TSRST_n
IO_L10P_T1_D14_14	M24	CPU TRST_n
IO_L10N_T1_D15_14	M25	CPU TRICK
IO_L11P_T1_SRCC_14	L22	CPU TTDI
IO_L11N_T1_SRCC_14	L23	CPU TTMS
IO_L12P_T1_MRCC_14	M21	CPU TTCK
IO_L12N_T1_MRCC_14	M22	R150 22 SPI SCLK
IO_L13P_T2_MRCC_14	N21	SEG_PD
IO_L13N_T2_MRCC_14	N22	SEG_PE
IO_L14P_T2_SRCC_14	P20	FPGA_USB0_LOW
IO_L14N_T2_SRCC_14	P21	SEG_3V3_D0
IO_L15P_T2_DQS_RDWR_B_14	N23	LED7
IO_L15N_T2_DQS_DOUT_CSO_B_14	N24	LED6
IO_L16P_T2_CSI_B_14	P19	LED5
IO_L16N_T2_A15_D31_14	N19	LED4
IO_L17P_T2_A14_D30_14	P23	SEG_PG
IO_L17N_T2_A13_D29_14	P24	SEG_DP
IO_L18P_T2_A12_D28_14	R20	I2C_SCL
IO_L18N_T2_A11_D27_14	R21	I2C_SDA
IO_L19P_T3_A10_D26_14	R25	SEG_3V3_D1
IO_L19N_T3_A09_D25_VREF_14	P25	FPGA_USB0_FULL
IO_L20P_T3_A08_D24_14	N26	FPGA_USB0_P
IO_L20N_T3_A07_D23_14	M26	FPGA_USB0_N
IO_L21P_T3_DQS_14	T24	SEG_PF
IO_L21N_T3_DQS_A06_D22_14	T25	FPGA_USB1_FULL
IO_L22P_T3_A05_D21_14	R26	FPGA_USB1_P
IO_L22N_T3_A04_D20_14	P26	FPGA_USB1_N
IO_L23P_T3_A03_D19_14	T22	FPGA_USB0_PWR_DET
IO_L23N_T3_A02_D18_14	R22	FPGA_USB0_PWR_EN
IO_L24P_T3_A01_D17_14	T23	FPGA_USB1_PWR_EN
IO_L24N_T3_A00_D16_14	R23	FPGA_USB1_LOW
IO_25_14	R18	FPGA_USB1_PWR_DET

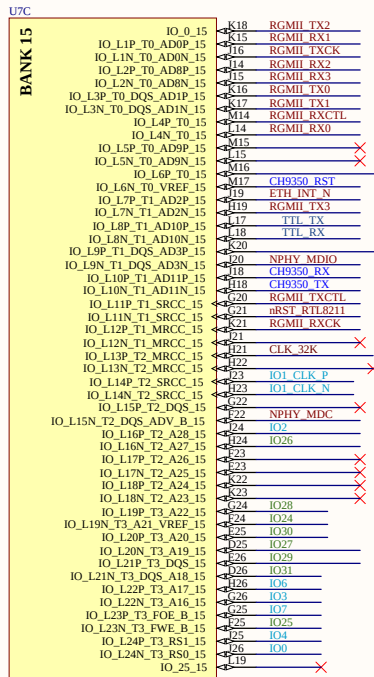
XC7A100T-2FGG676I



changed SEG_PF with SEG_3V3_D0

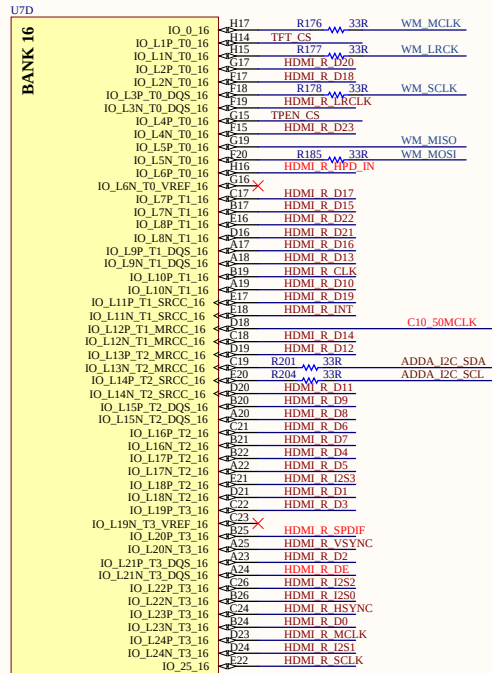
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Date: 2021-07-05 Time 6:06:50 PM	Engineer: RJWG
Revision: DDRV1.0	Sheet 08 of 25
	Size: A4

BANK15 3.3V

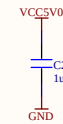
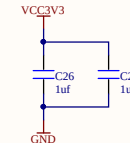
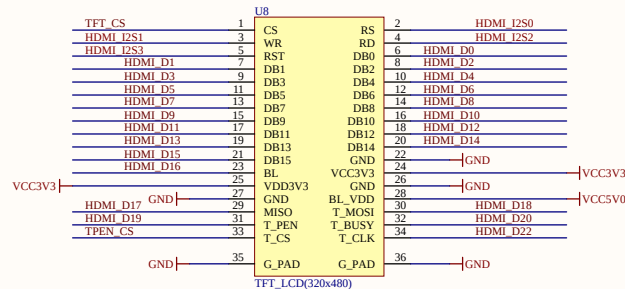
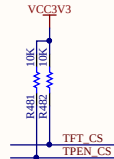
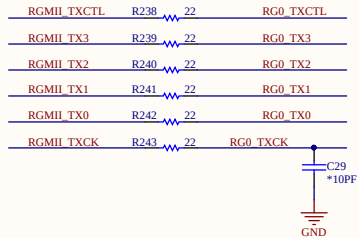
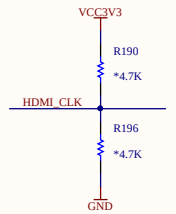
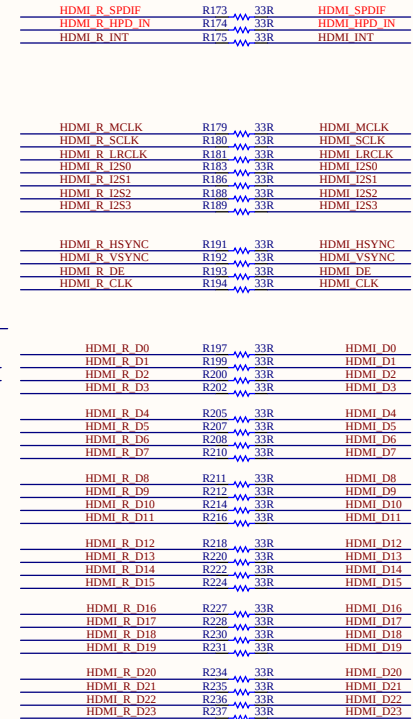


XC7A100T-2FGG676I

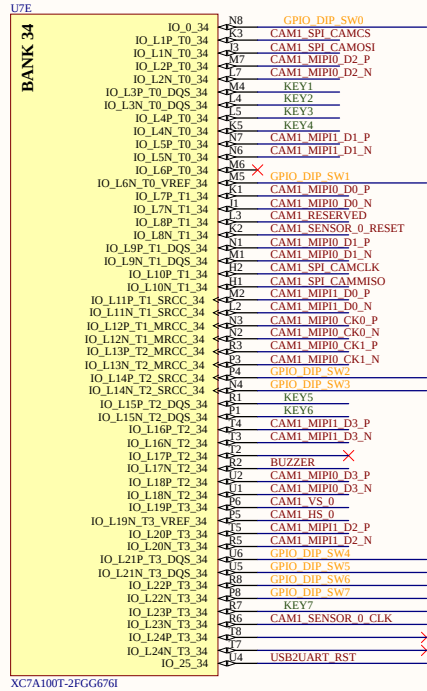
BANK16 3.3V



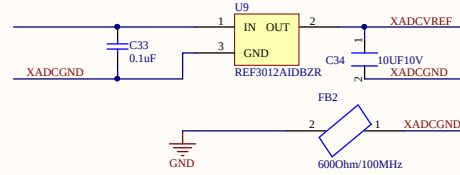
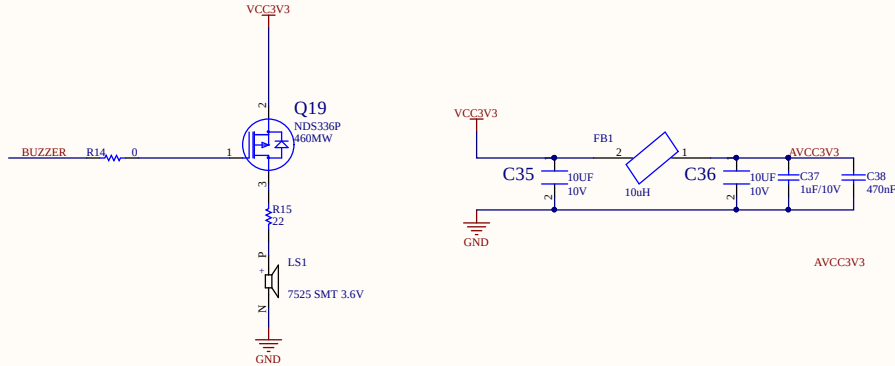
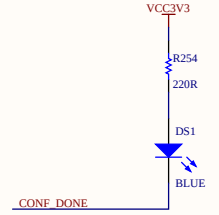
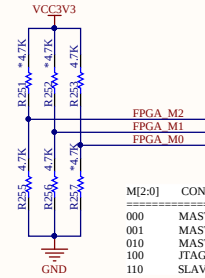
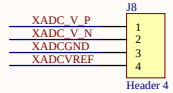
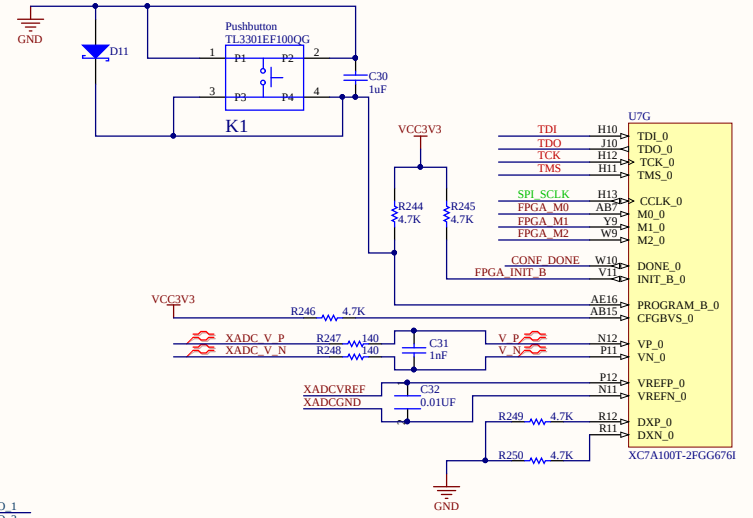
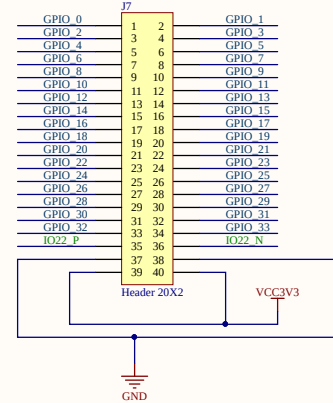
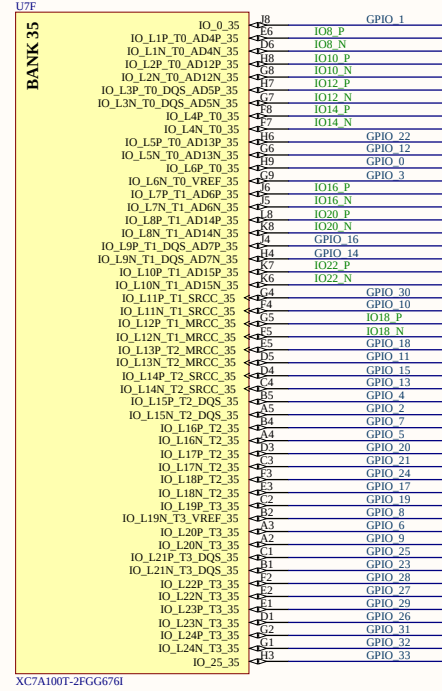
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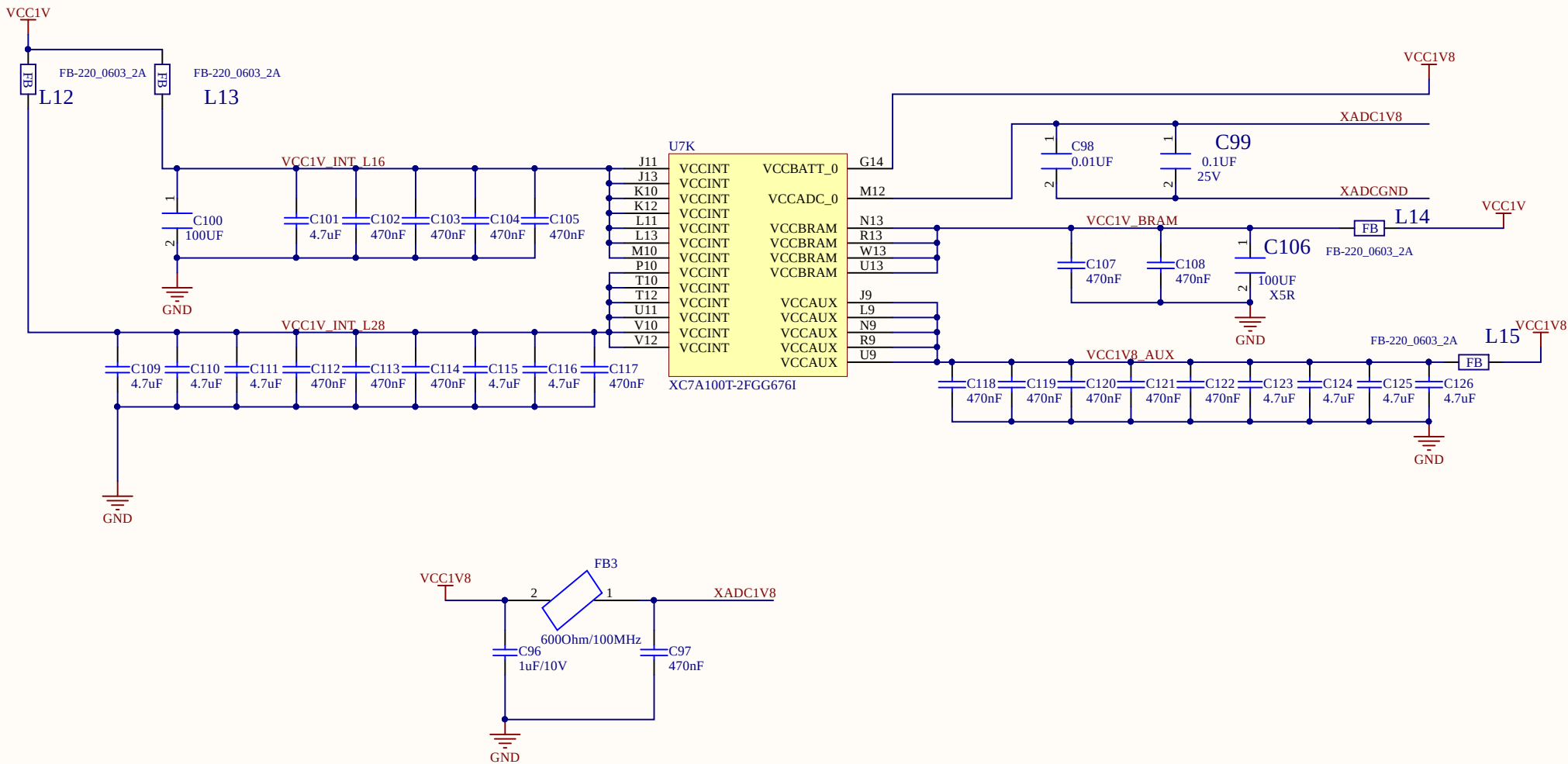


BANK34 1.8V/3.3V

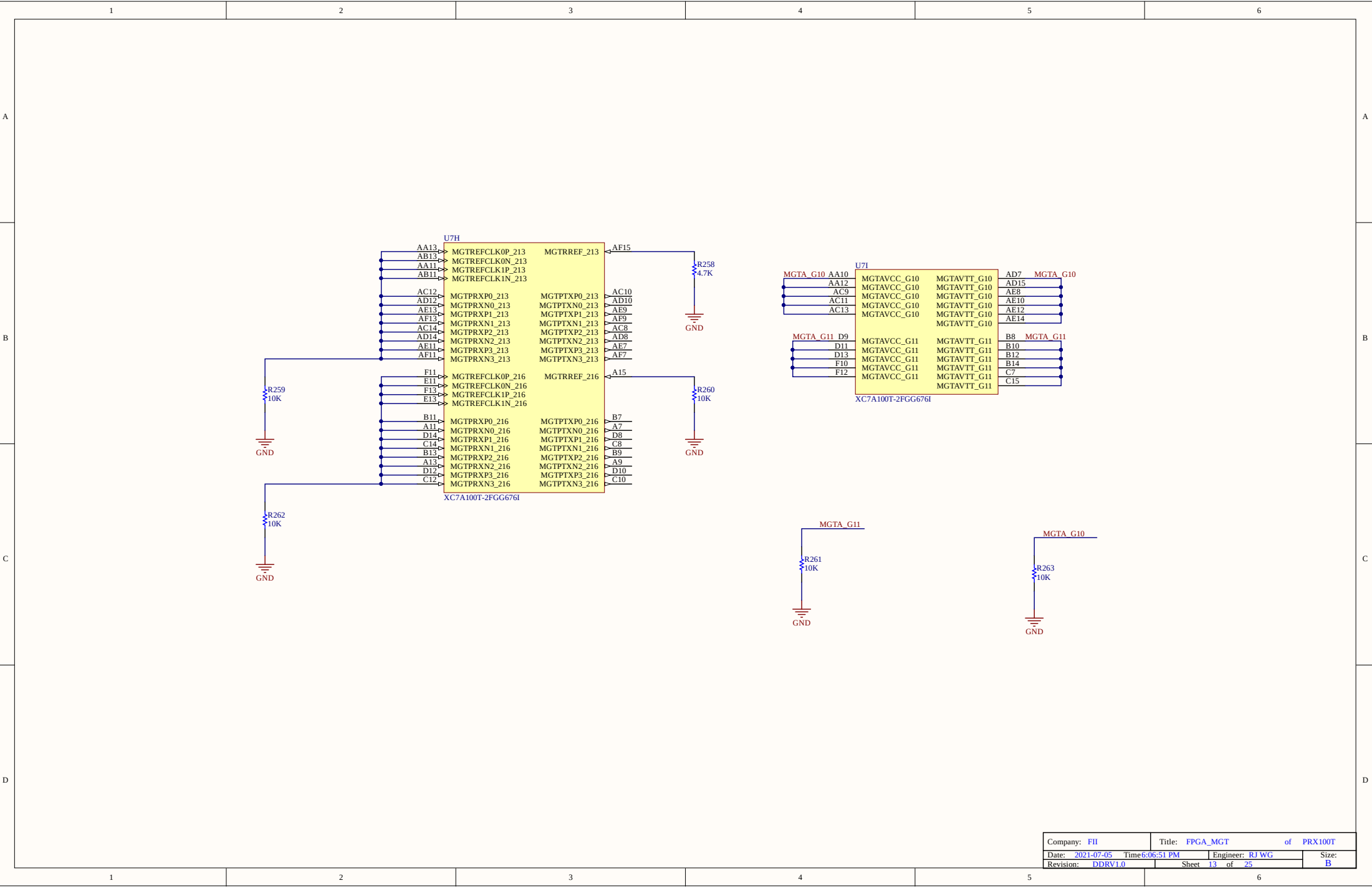


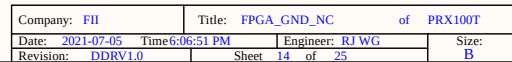
BANK35 1.8/3.3V

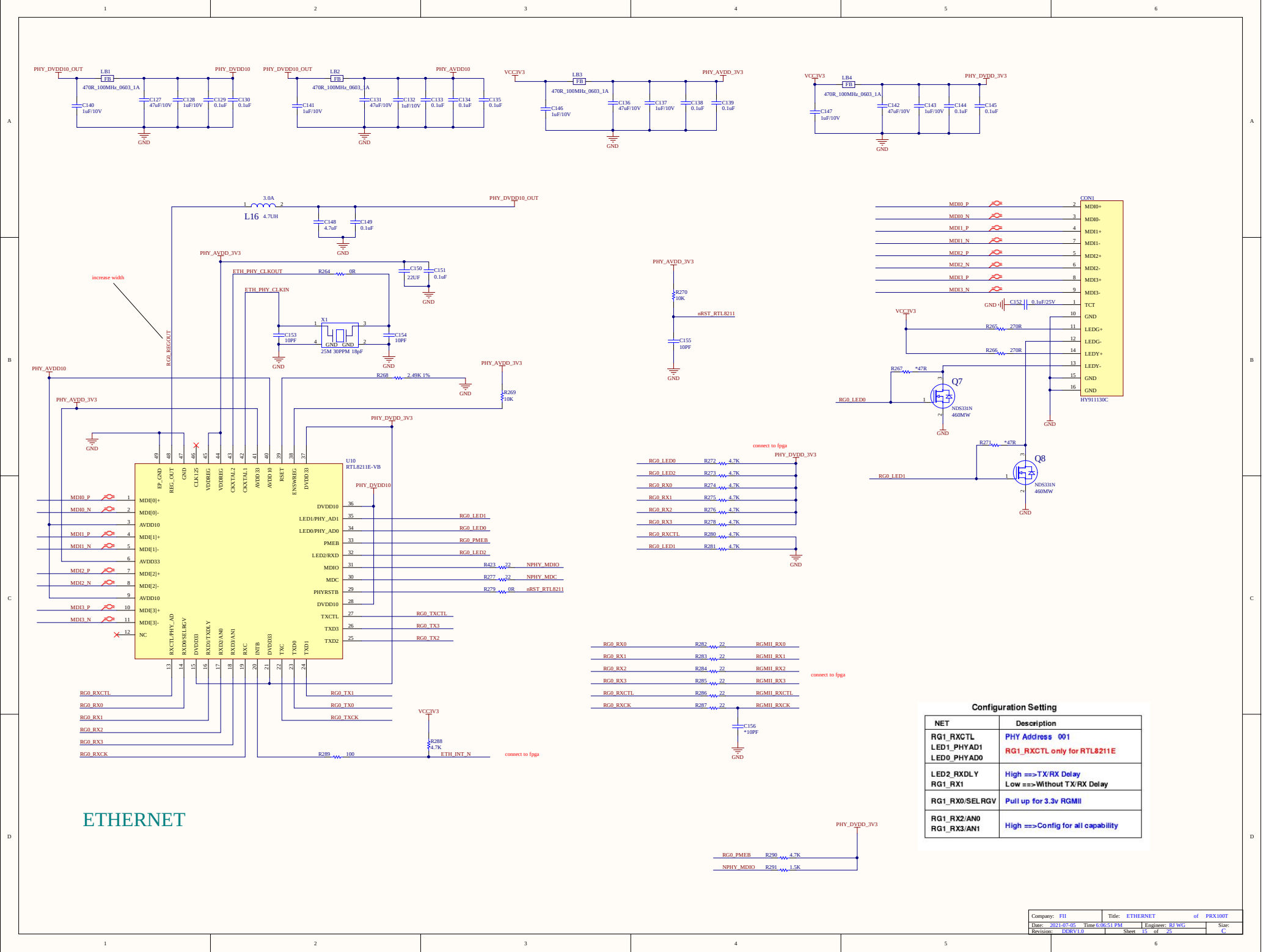




Company: FII		Title: FPGA_CORE_POWER of PRX100T	
Date: 2021-07-05	Time: 6:06:51 PM	Engineer: RJWG	Size: A4
Revision: DDRV1.0	Sheet 12 of 25		



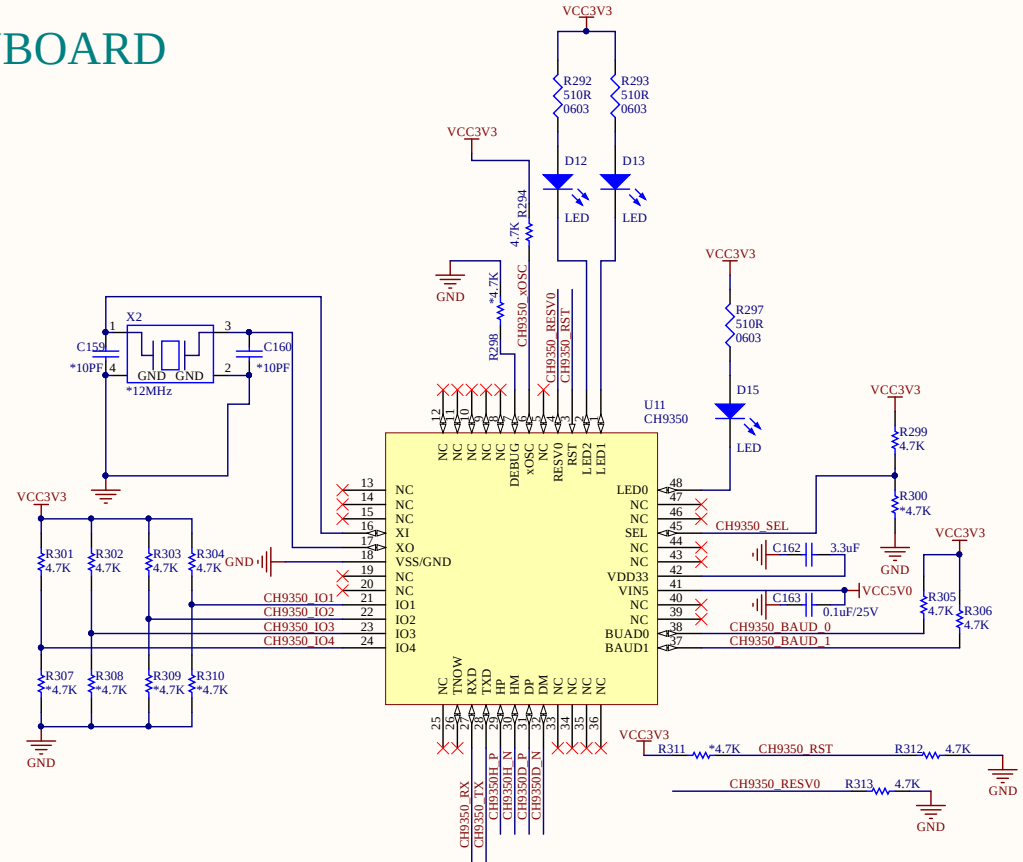
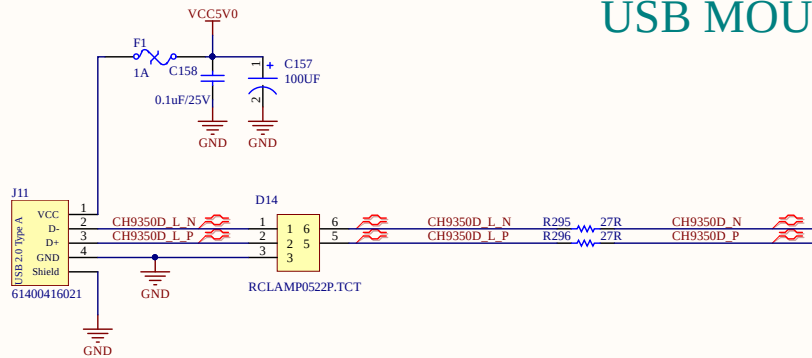




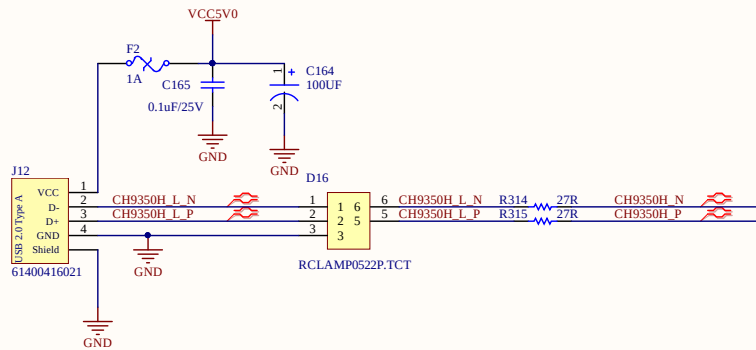
ETHERNET

Configuration Setting	
NET	Description
RG1_RXCTL LED1_PHYAD1 LED0_PHYAD0	PHY Address 001 RG1_RXCTL only for RTL8211E
LED2_RXDLY RG1_RX1	High ==> TX/RX Delay Low ==> Without TX/RX Delay
RG1_RX0/SELRGV	Pull up for 3.3v RGMII
RG1_RX2/AN0 RG1_RX3/AN1	High ==> Config for all capability

USB MOUSE/KEYBOARD

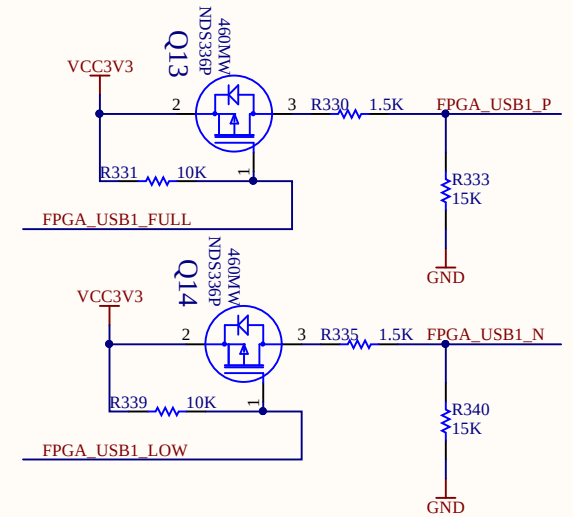
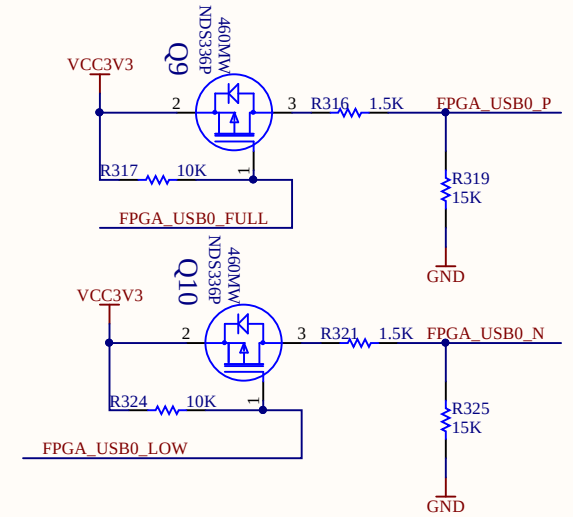
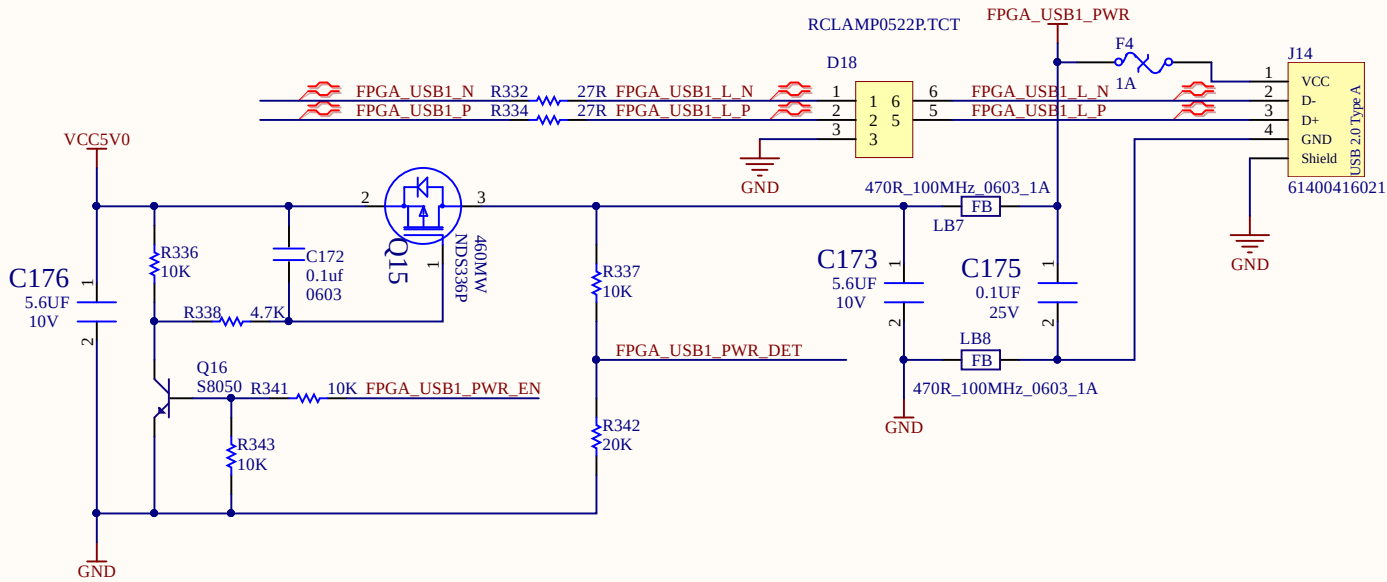
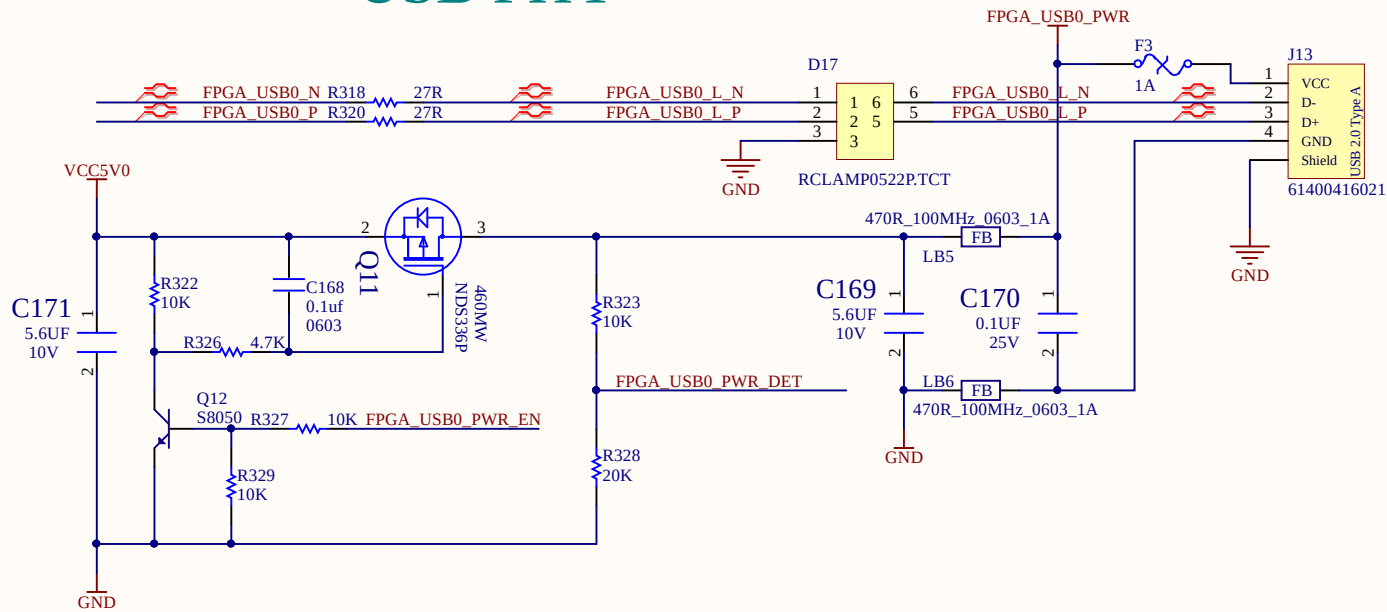


USB DEVICE TO UART



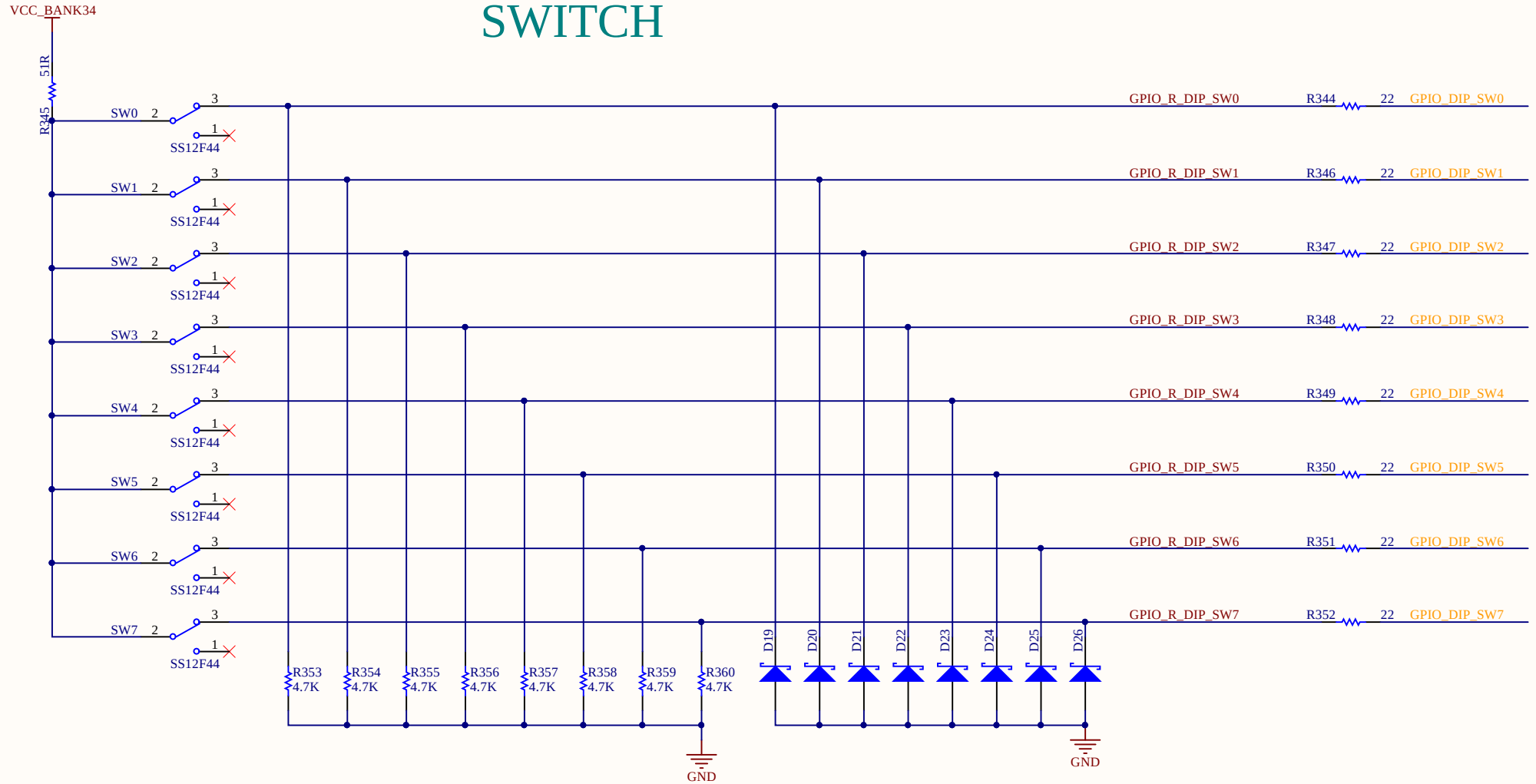
Company: FH	Title: USB	of PRX100T
Date: 2021-07-05	Time: 6:06:51 PM	Engineer: RJ WG
Revision: DDRV1.0	Sheet 16 of 25	Size: B

USB PHY



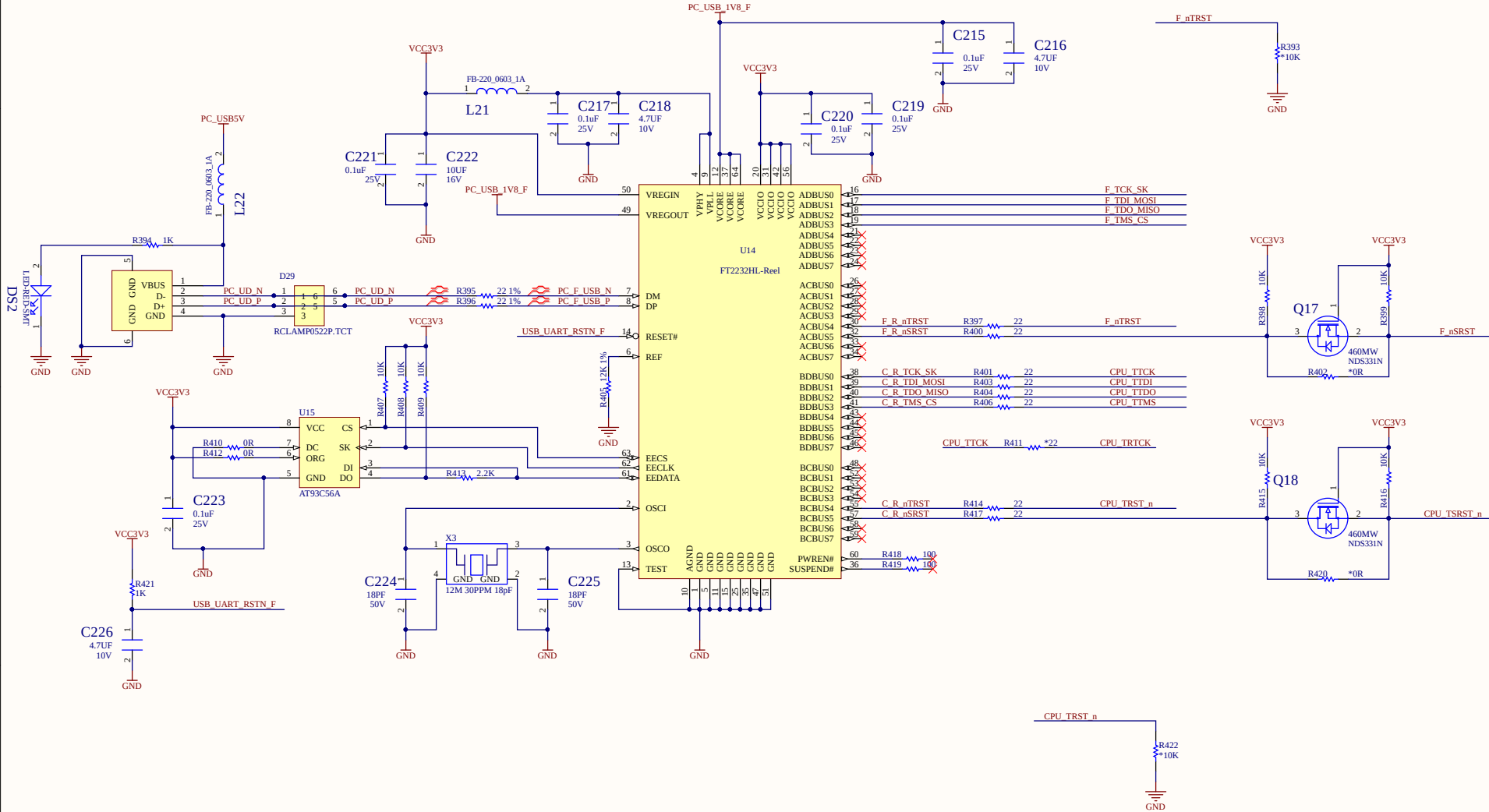
Company: FII	Title: USB_FPGA	of PRX100T
Date: 2021-07-05	Time: 6:06:52 PM	Engineer: RJ WG
Revision: DDRV1.0	Sheet 17 of 25	Size: A4

SWITCH



Company: FII	Title: SW	of PRX100T
Date: 2021-07-05	Time: 6:06:52 PM	Engineer: RJWG
Revision: DDRV1.0	Sheet 18 of 25	Size: A4

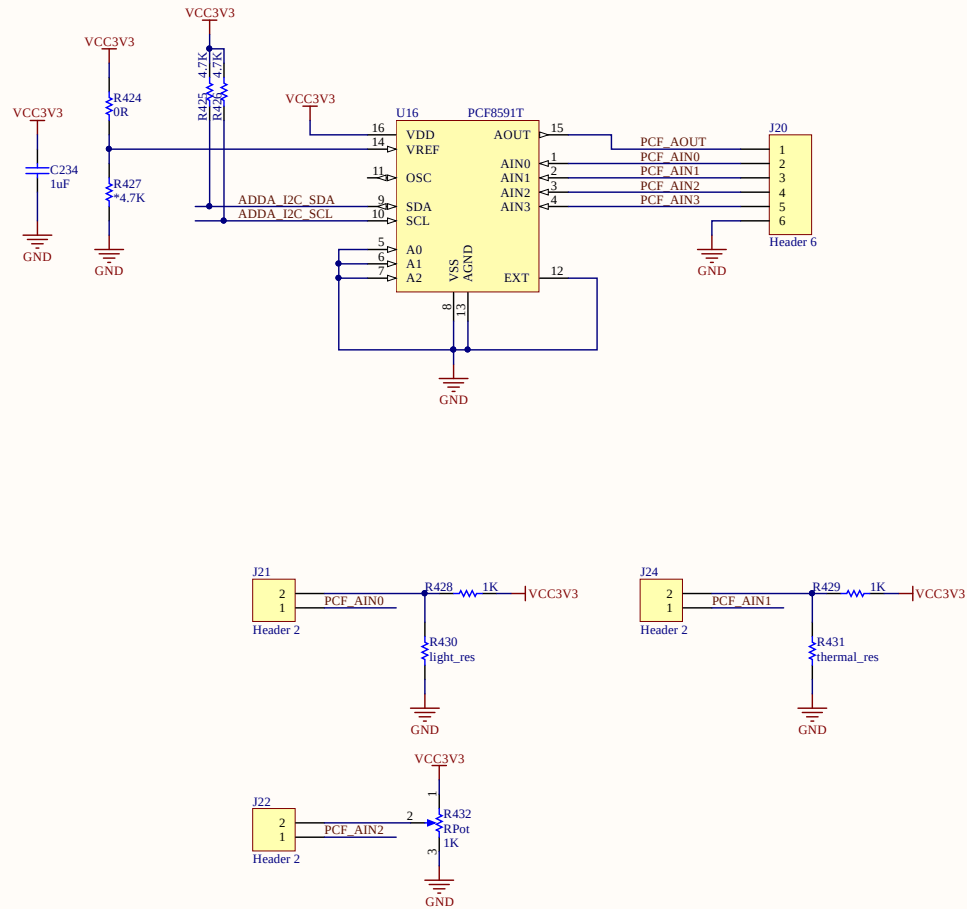
JTAG/UART



AUDIO WM8978

AUDIO WM8978

AD/DA



Company: FH	Title: AD_DA of PRX100T		
Date: 2021-07-05	Time: 6:06:53 PM	Engineer: RJ WG	Size: B
Revision: DDRV1.0	Sheet 23	of 25	

PL DDR3 MEMORY

